Figures 50 and 51 are diagrams that illustrate the building of a packet queue in connection with the operation of the embodiment of Figure 48.

Figure 52 is a diagram that illustrates a technique for accessing certain information stored in external memory in a reduced amount of time in connection with the embodiment of Figure 48.

Figure 53 is a diagram that illustrates a serial bus that couples an egress MS-SAR of a line card to an ingress MS-SAR of the same line card. The egress MS-SAR can use the serial bus to backpressure the sending ingress MS-SAR.

Figure 54 is a block diagram on one particular embodiment of incoming SPI-4 interface block 201 of Figure 10.

Figure 55 is a diagram of input control block 801 of Figure 54.

Figure 56 is a diagram of output control block 803 of Figure 54.

Figure 57 is a block diagram of one particular embodiment of segmentation block 203 of Figure 10.

Figure 58 is a block diagram of one particular embodiment of memory manager block 204 of Figure 10. Figures 58A and 58B together form a more detailed version of Figure 58.

Figure 59 is a block diagram of one particular embodiment of reassembly block 205 of Figure 10. Figures 59A-59D together form a more detailed version of Figure 59.

Figures 60A-60J are diagrams that illustrate reassembly types carried out by the reassembly block of Figure 59. The function of the reassembly block in each of these reassembly types can be described at the functional level in Verilog, and hardware circuitry realized from the Verilog using hardware synthesis software.

Figure 61 is a diagram of one particular embodiment of outgoing SPI-4 interface block 206 of Figure 10. Figures 61A and 61B together form a more detailed version of Figure 61.

Figure 62 is a diagram of CPU interface block 211 of Figure 10.

DETAILED DESCRIPTION

Figure 4 is a simplified diagram of a router 100 in accordance with an embodiment of the present invention. Router 100 includes a plurality of line cards